CLAIMS

1. An A/D conversion array comprising arrayed unit circuits, each of which comprising:

a circuit element for performing N-bits of A/D conversion per cycle;

a circuit element for D/A converting the digital output of said circuit element by first switching means and a first capacitor;

amplification means for connecting a second capacitor for determining gain by a ratio with said first capacitor between the input and output of an inverting amplifier for subtracting the analog value of said conversion result from the analog input and for amplification of the analog input;

a circuit element for sampling and holding the output of said amplification means by second switching means and said first capacitor; and

third switching means for selecting one of output of said amplification means and an input signal and supplying the selected signal to said amplification means as input, via said first capacitor, the A/D conversion array being characterized in that

control means for said first to third switching means is installed outside the array, an input signal is

supplied as the input of said amplification means in the first stage, and a signal through said sample and hold circuit element is supplied to the input of said amplification circuit in the next stage, whereby cyclic multi-bit A/D conversion is performed.

2. The A/D conversion array according to Claim 1, characterized in that two first capacitors used for D/A conversion by said amplification means are installed, and the conversion speed per cycle is doubled by alternately using said plurality of capacitors for D/A conversion and for sampling and holding.

3. The A/D conversion array according to Claim 1, characterized in that said circuit element for performing N-bits of A/D conversion divides the analog signals, which are input, into three areas depending on a voltage level, and assigns the values 1, 0 and -1 to the three areas.

4. The A/D conversion array according to Claim 1, characterized in that an amplifier in said amplification means is a differential amplifier having a differential input and a differential output, and a full differential circuit is structured by said differential amplifier, and a capacitor and switching means in the peripheral area thereof.

5. An image sensor, characterized by performing A/D conversion in parallel for the output of an image sensor array by arranging the A/D conversion array according to Claim 1 to Claim 4 in a column of the image sensor array.

6. The image sensor according to Claim 5, further comprising a noise cancellation circuit in a column of said image sensor array, characterized in that said noise cancellation circuit comprises a second inverting amplifier, a third capacitor connected between the output of the image sensor array and the input of said second inverting amplifier, and a fourth capacitor connected between the input and output of said second inverting amplifier, and switching means for switching connections of these elements, and the inverting amplifier in said cyclic A/D conversion array is also used as the second inverting amplifier of said noise cancellation circuit, said first capacitor is also used as said third capacitor, and said second capacitor is also used as said fourth capacitor.

7. The image sensor according to Claim 6, further comprising a fifth capacitor as a capacitor to be connected between the output of the image sensor array and input of the inverting amplifier only during a noise cancellation operation, characterized in that an amplification function is acquired by the capacity ratio with said second capacitor.